CDB5364

Evaluation Board for CS5364

Features

- Single-Ended to Differential Analog Inputs
- 3.3 V Logic Interface
- Connection for DSP Serial I/O
- Windows®-Compatible CDB5364 Software Supplied by Cirrus to Configure the CS5364
- On-Board CS8406 to Generate S/PDIF and EIAJ-340 Digital Audio
- Requires Only an Analog Signal Source, Power Supplies and, optionally, a PC for a Complete Analog-to-Digital-Converter Evaluation System

Description

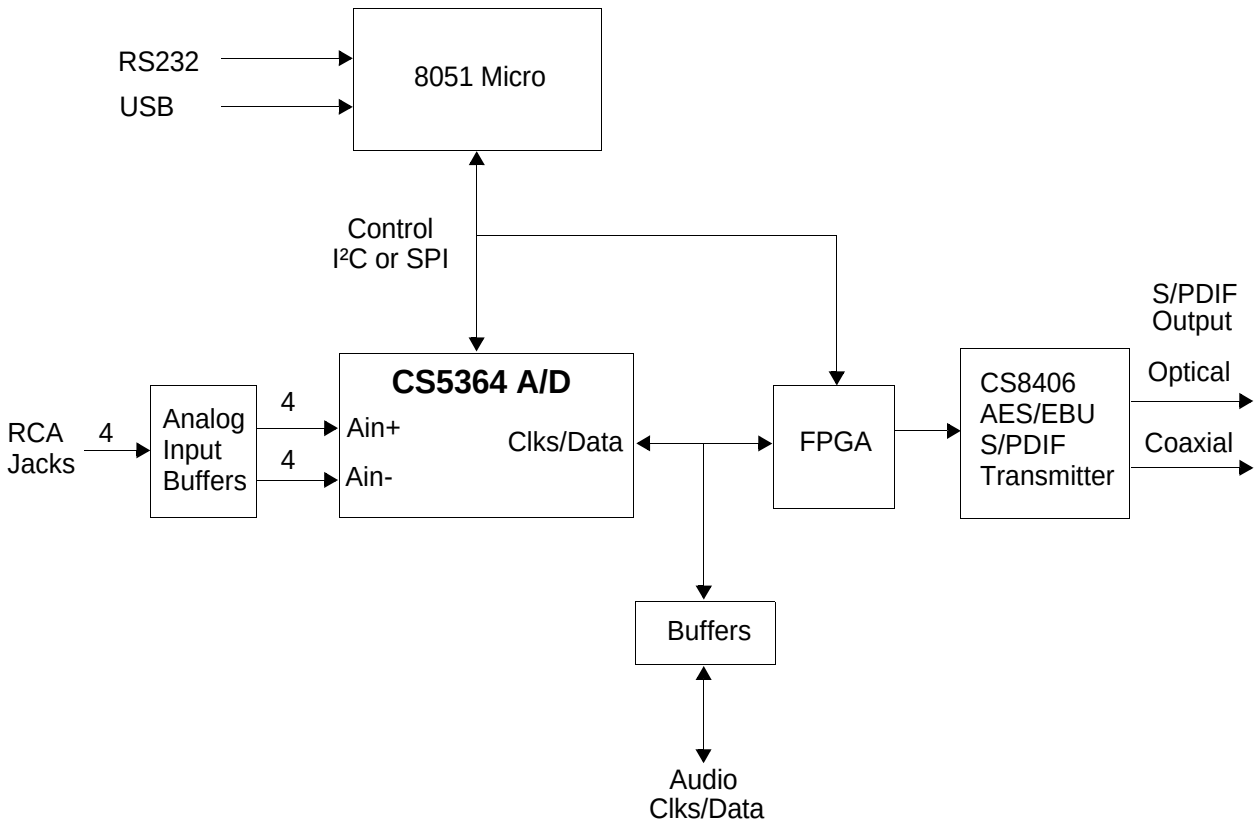
The CDB5364 evaluation board is an excellent means for quickly evaluating the CS5364 24-bit, 192 kHz A/D converter. Evaluation requires only a digital signal analyzer, an analog signal source, and a power supply.

On-board DIP switches configure the CS5364 in Stand-Alone mode, avoiding the need for a PC.

For software-based device configuration, the Control Port mode is used by attaching a host PC to the Evaluation Board and executing the provided FlexGUI software.

ORDERING INFORMATION

CDB5364 Evaluation Board



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1. CDB5364 SYSTEM OVERVIEW

The CDB5364 Evaluation Board provides an excellent means of quickly evaluating the CS5364. A digital audio interface transmitter (CS8406) provides an easy interface to digital audio signal analyzers, including the majority of digital audio test equipment. Standard analog input and digital output connectors are included for quick and reliable board setup. An on-board FPGA is used for configuring the various modes of the CS5364. Graphical User Interface software is supplied by Cirrus Logic, which allows programming the CDB5364 when connected to a host PC running Microsoft Windows®.

2. QUICK-START GUIDE

- Confirm that DIP switches S1 and S4 are in the closed (LO) position, pushed down to the right.
- Connect the following jumpers.
  - J7 - Install 5 jumpers to the left side of J7, enabling the DIP switches to operate correctly.
  - J81, J95 - Install jumpers to these positions, grounding XTI and XTO of the CS5364.
  - J1 - Install a jumper at the +5 V position, allowing VA to be supplied by the +5 V supply.
- Install a 12.288 MHz canned Oscillator to socket Y1, providing a Master Timing Clock for the system.
- Install a jumper to J11 at the OSC position to enable the OSC drive buffer.
- Connect power supply common to the GND binding post. Connect +5 V, +12 V and -12 V to the binding posts as marked on the board silkscreen

This configuration provides a completely operational 24-bit Analog-to-Digital-Converter evaluation system. The CS5364 is operating as a Master Device in Single Speed Mode with a 48 kHz sampling rate. Apply power and connect analog input signals of 1 Vrms maximum (full scale) to the RCA inputs jacks. S/PDIF Digital audio data is available for evaluation at the Optical and Coaxial outputs.

3. DETAILED BOARD FEATURES

The CDB5364 Evaluation Board supports both the Stand-Alone and Control Port modes of the CS5364. An FPGA (U2) controls digital signal routing between the CS5364, the CS8406 and the DSP I/O header. For user-friendly evaluation of the TDM interface, the FPGA will translate TDM data into PCM data and send it to the CS8406.

3.1 Stand-Alone Evaluation

In Stand-Alone mode, the CDB5364 runs without an external PC attached. In this mode, the FPGA controls operation of the board by dynamically reading DIP switches (S1 and S4) after a cold power-up or a push-button board reset. Stand-Alone mode provides the most commonly used device settings. For additional control of the CS5364, Control Port mode is used.

In Stand-Alone mode, as the DIP switches are repositioned, the FPGA simultaneously sets the appropriate pins on the CS5364 and CS8406 to keep them synchronized with regard to sampling speed and data format.

3.1.1 S1 and S4 Switch Operation

DIP Switch S1 contains six switches that function as described below.

M1,M0 set the device Speed Mode
- 0x00 Single Speed Master
- 0x01 Double Speed Master
- 0x10 Quad Speed Master
- 0x11 Slave all speed

DIF1,DIF0 set the Digital Audio Interface Data format
- 0x00 Left Justified
- 0x01 I²S
- 0x10 TDM 2-wire
- 0x11 TDM 4-wire

TDM1 and TDM0 support both TDM mode and PCM mode.

In TDM mode, TDM1 and TDM0 select two stereo pairs from a TDM stream, convert the data to Left-Justified PCM format then send the data to the CS8406 S/PDIF transmitter.
- 0x00 TDM Pair 1 (Channel 1, 2)
- 0x01 TDM Pair 2 (Channel 3, 4)
- 0x1x Reserved

In PCM mode, TDM1 and TDM0 select which SDOUT is sent to the CS8406.
- 0x00 SDOUT1 (Channel 1, 2)
- 0x01 SDOUT2 (Channel 3, 4)
- 0x1x Reserved

DIP Switch S4 contains two switches which function as described below.7

MDIV - divides the master clock by 2 when OPEN (HI).
CLKMODE - divides the master clock by 1.5 when OPEN (HI)

3.2 Control-Port Evaluation

The CDB5364 is shipped with a Cirrus Logic designed Microsoft Windows-based program that allows full control over the CS5364 internal registers. This software program is called the FlexGUI, and it is loaded by executing the FlexLoader.exe file. Hardware interface to the FlexGUI is provided by connecting an RS-232 cable or a USB cable between a host PC and the CDB5364. Once the FlexGUI is loaded, the Evaluation Board DIP switches are ignored, and all register settings are available for reading and writing using software control. Testing configurations may be quickly reproduced by using the FlexGUI to save and restore unique register settings.

Configure the board for Control Port operation using the instructions that follow.

- Connect jumpers.
  - J7 - Install 5 jumpers to the left side of J7, enabling the I²C control interface.
  - J81, J95 - Install jumpers to these positions, grounding XTI and XTO of the CS5364.
  - J9 - Install a jumper at the +5 V position, allowing VA to be supplied by the +5 V supply (VA may be externally supplied at the VA binding post by moving jumper J9 to the VA EXT position).
- Add an oscillator of choice to socket Y1 to provide a Master Timing Clock for the system. A crystal may also be used by removing the canned oscillator and jumpers J81, J95 and J11. The CDB5364 Evaluation Board is shipped with 39 pF loading capacitors for crystal-based oscillators. Soldering pads are provided on the board for users that require third overtone tank circuit operation or different loading capacitors.
- Connect the power supply common to the GND binding post. Connect +5 V, +12 V and -12 V to the binding posts as marked on the board silkscreen.

The FlexGUI provides two convenient views of the CDB5364 Evaluation Board settings. The default view is a high-level functional mapping of settings. The second view is a lower-level register map view for programming at the bit level. Each view is synchronized with the other view, so that changing a setting at one level will also change the corresponding setting in the alternate level.

3.3 FlexGUI Hi-Level View

The Cirrus Logic FlexGUI defaults to the Hi-Level View as shown in Figure 1. This view provides functionally grouped control over the CS5364, reducing the need to memorize the exact location of bit settings. Any register may be modified at any time; however, the effect of changes made to the CS5364 is gated off until the Control Port Bit is enabled.

When switching to TDM mode, the CS8406 Clock and Date source (Board Control Panel) must be changed prior to changing the CS5364 SAI format. This sequential ordering resets the FPGA to assure that it timed properly with the CS5364 TDM packet stream.

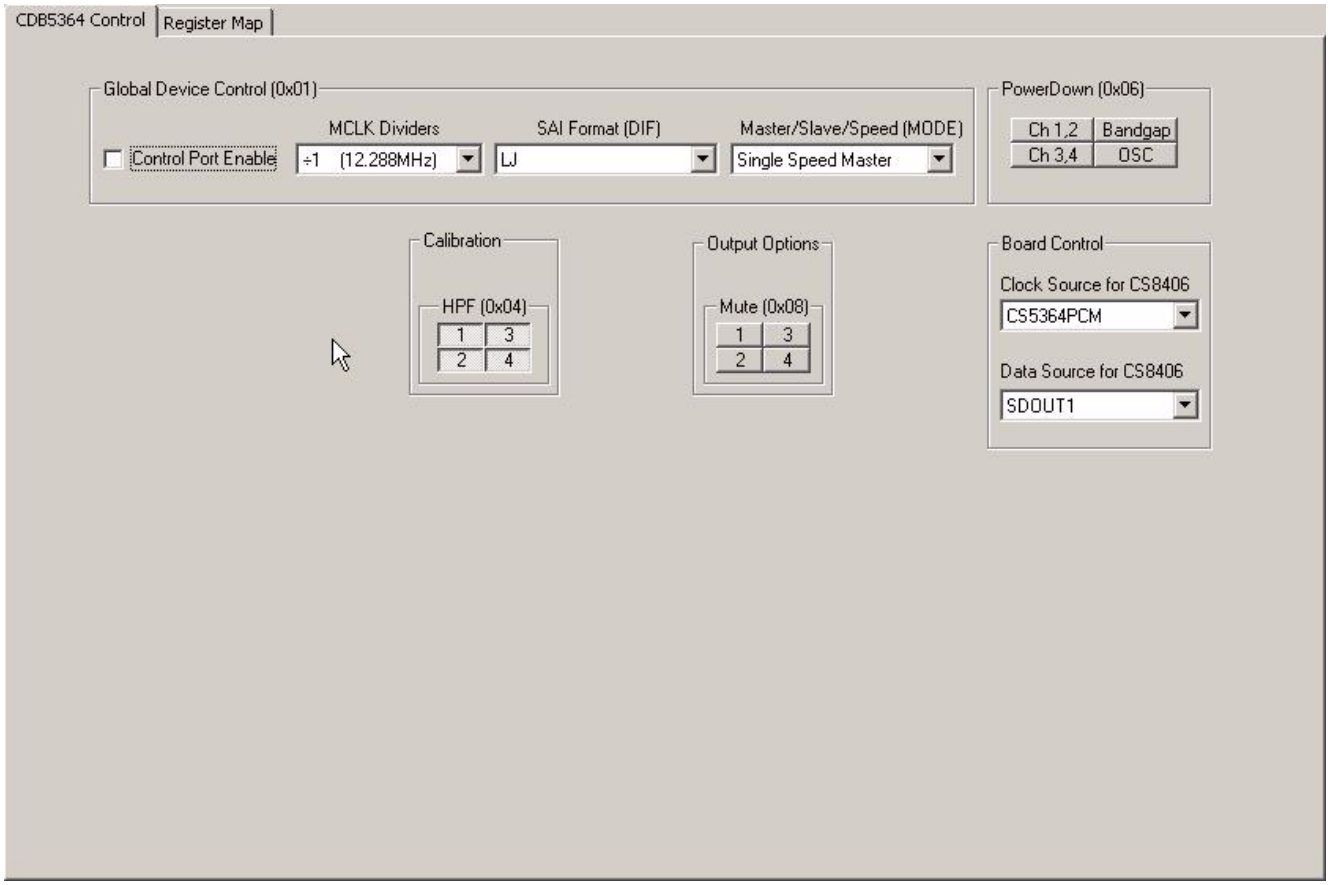

Figure 1. Hi-Level FlexGUI View

3.4 FlexGUI Low-Level View

The Low-level Register Map view provides direct control over the CS5364, the FPGA and GPIO settings that change the CS5364 device address. Select the desired device tab; then select and modify any write-register values. Register modification is always a READ-WRITE-READ operation and is usable at both the byte or bit level. For byte-level control, type the required hex value in the desired register field numerical box. For bit-level control, click the corresponding graphical push-button in the desired register field or use the pull-down menu to access and change the bit values.

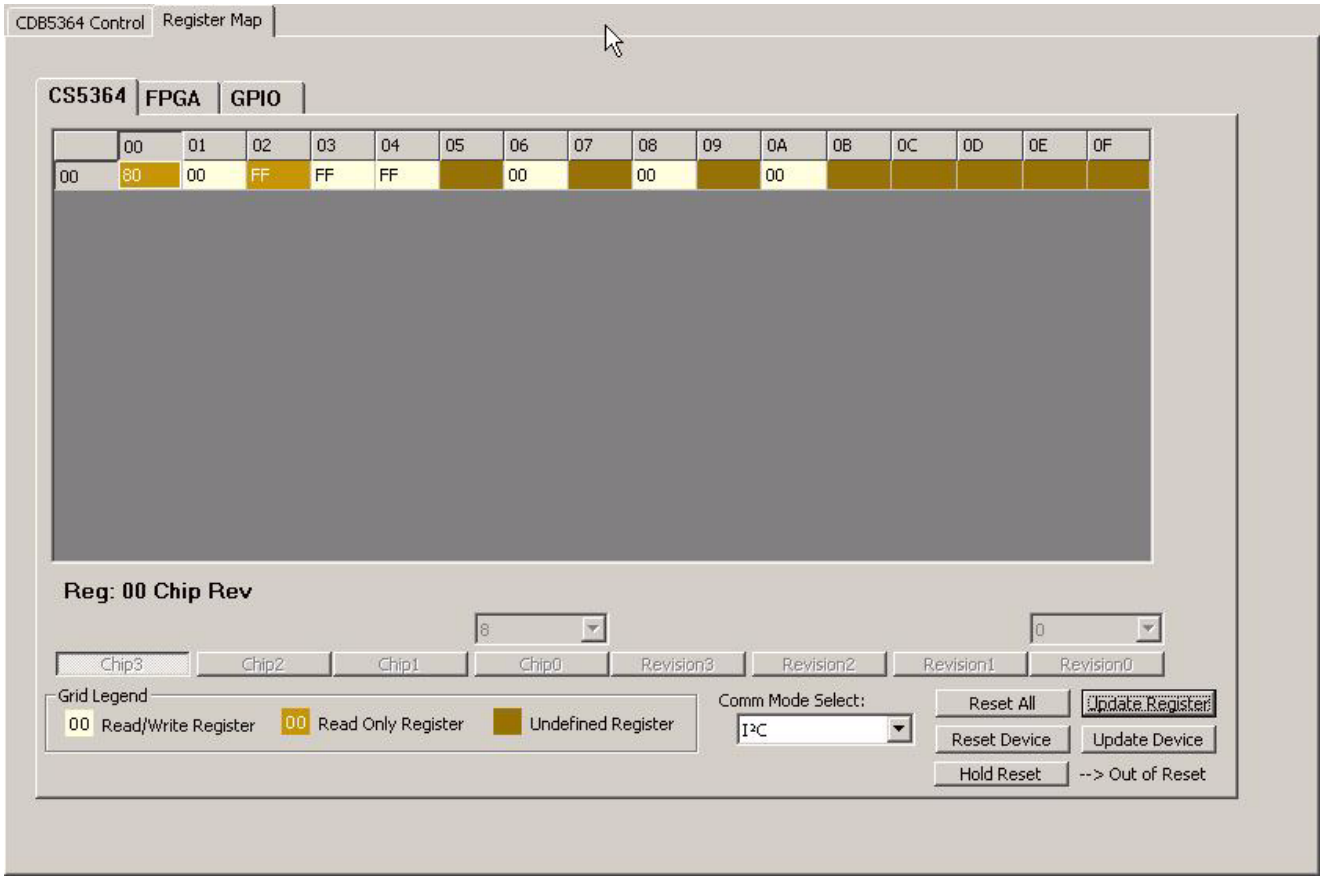

Figure 2. FlexGUI Low-Level Register View

When the CS5364 is put in Control Port mode, the DIP switches are ignored and configuration is determined by the register bits. When placed back in Stand-Alone mode, the DIP switches regain board control. Exiting Control Port mode is achieved by stopping the FlexGUI program. Once the program is stopped, about three seconds later, Stand-Alone mode is established.

3.5 Bit Definitions

3.5.1 CS5364 Bits

The Low-Level view of the FlexGUI provides the full register set of the CS5364 under the CS5364 tab. The CS5364 datasheet provides full details of internal register operation.

3.5.2 FPGA Bits

FPGA Register 0x00 is non-functional and only contains the revision code of the FPGA.

FPGA Register 0x01 is a functional register that provides the following functionality.

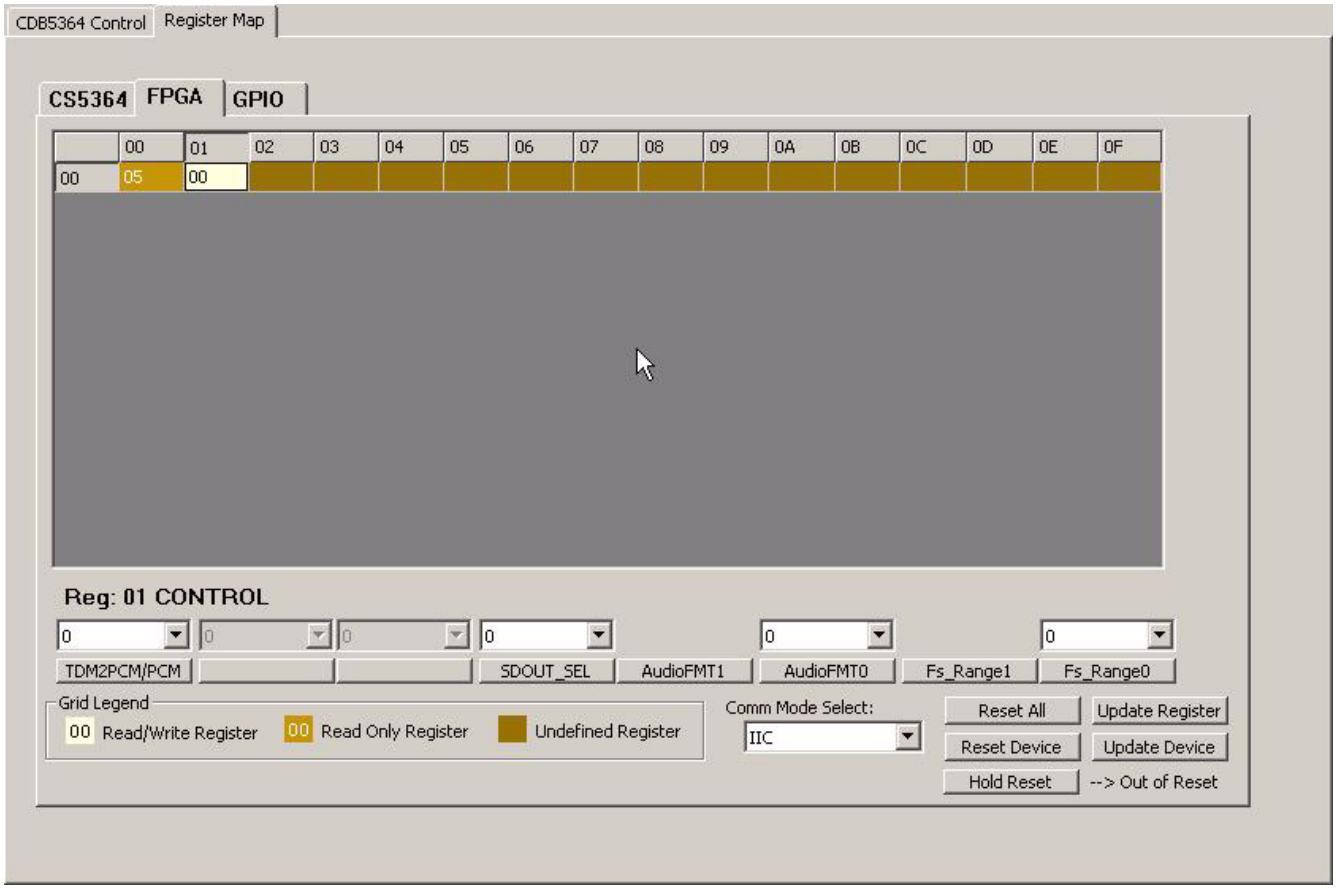

Figure 3. FPGA Low-Level Bit View

Fs_Range1,0 set the device Speed Mode. These bits need to be changed when using the Serial Audio Interface of the DSP header to communicate with external equipment.

0x00 Single Speed Master
0x01 Double Speed Master
0x10 Quad Speed Master
0x11 Slave all speed

AudioFMT1,0 set the Serial Audio Interface format when attaching the Serial Audio Interface of the DSP header to external equipment.

0x00 Left Justified
0x01 I²S
0x10 TDM 2-wire
0x11 TDM 4-wire

In TDM mode, SDOUT_SEL1 and SDOUT_SEL 0 extract two stereo pairs from the CS5364 TDM stream, convert the data to Left-Justified PCM format and send the data to the CS8406 data input pin.

0x00 TDM Pair 1 (Channel 1, 2)
0x01 TDM Pair 2 (Channel 3, 4)
0x1x Reserved

In PCM mode, SDOUT_SEL1 and SDOUT_SEL 0 select which SDOUT pin of the CS5364 is sent to the CS8406.

0x00 SDOUT1 (Channel 1, 2)
0x01 SDOUT2 (Channel 3, 4)
0x1x Reserved

TDM2PCM/PCM selects the clock source for the CS8406.

0x00 8406 Clock Source is CS5364
0x01 8406 Clock Source is the FPGA TDM2PCM engine

4. CDB5364 HARDWARE

The CDB5364 Evaluation Board has a number of connections, switches and jumpers that provide ease and convenience for quickly evaluating the most commonly used functions of the CS5364 silicon device. The following tables list the purpose of each hardware option on the Evaluation Board.

4.1 Input and Output Connectors

The input and output connectors provide power and signal connectivity to the CDB5364 Evaluation Board as shown in Table 1.

DESIGNATOR	NAME	CLASS	FUNCTION
J6	GND	Ground	Ground connection from power supply
J2	+5 V	Power	+ 5 Volt power for CS5364
J16	+12 V	Power	+12 V power for the active input buffers
J17	-12 V	Power	-12 V power for the active input buffers
J20	AIN1	Analog Input	Analog input channel 1
J21	AIN2	Analog Input	Analog input channel 2
J22	AIN4	Analog Input	Analog input channel 4
J23	AIN3	Analog Input	Analog input channel 3
OPT1	Optical Output	Digital Output	S/PDIF Optical Digital audio output
J3	Coax Output	Digital Output	S/PDIF Coaxial Digital audio output
J5	RS232 I/O	Digital I/O	FlexGUI Interface port to PC
J10	USB I/O	Digital I/O	FlexGUI Interface port to PC

Table 1. CDB5364 Input and Output Connectors

4.2 Switches

The CDB5364 Evaluation Board switches are used for setting speed modes and format protocols and for resetting devices to their default state. The switch functions are described in Table 2.

DESIGNATOR	NAME	FUNCTION (see CS5364 Datasheet for details)
S1-1	M0	speed mode; Master/Slave function
S1-2	M1	speed mode; Master/Slave function
S1-3	DIF0	Data Format
S1-4	DIF1	Data Format
S1-5	TDM0	Select Channel pairs for S/PDIF output
S1-6	TDM1	Select Channel pairs for S/PDIF output
S4-1	MDIV	Master Clock Divider
S4-2	CLKMODE	Master Clock Divider
S3	BOARD RESET	Resets CS5364, CS8406 and FPGA
S2	PGM	Forces FPGA to be loaded with new code (not needed by user)

Table 2. CDB5364 Switches

4.3 User Configuration Jumpers

The CDB5364 Evaluation Board jumpers are used for signal routing as shown in Table 3

DESIGNATOR	NAME	FUNCTION
J7	CONTROL	Select I²C control Source
J91	-	Short to ground when not using Crystal
J85	-	Short to ground when not using Crystal
J11	OSC/XTL	Canned Oscillator/Crystal Selection
J9	+5 V/VA EXT	VA source selector
J4	DSP HEADER	

Table 3. User Jumpers

4.4 Reserved Factory Programming Jumpers

The CDB5364 Evaluation Board has two reserved headers, J15 and J8, that are used to factory program the Cygnal® 8051 microprocessor and the Xilinx® FPGA so that the FlexGUI interface operates correctly.

Caution! Do not apply power or shorts to these two jumpers as device damage could occur.

DESIGNATOR	NAME	FUNCTION
J15	MICRO_PROG	Reserved interface for pre-programming the Evaluation Board
J8	JTAG	Reserved interface for pre-programming the Evaluation Board

Table 4. CDB5364 Reserved Jumpers

4.5 Power Supply Circuitry

Power is applied to the evaluation board through five binding posts (+5 V, +12 V, -12 V, VA and GND). The GND connection is the common reference for power supplies. The +5 V binding post supplies digital power for all logic devices. The +12 V and -12 V binding posts supply power for the Operational Amplifier input buffers. The VA binding posts supplies power to the Analog Reference.

4.6 Grounding and Power Supply Treatment

As a high-peformance mixed-signal device, the CS5364 requires careful attention to power and grounding arrangements to optimize CS5364 performance. The CDB5364 Evaluation Board provides an excellent reference example of an optimum two-layer board layout that places decoupling capacitors as close to the CS5364 as possible and provides ground plane fill on both top and bottom layers.

4.7 FPGA Hardware

The on-board FPGA is utilized for several purposes. In addition to providing a method for configuring the CS5364 in Software mode, it contains its own configuration registers that provide clock and data routing for Master and Slave modes of the CS5364. The FPGA contains a multiplexer that selects which SDOUT line is routed to the CS8406. It also contains a TDM2PCM engine that extracts channel pairs from a TDM stream and sends them to the CS8406.

4.8 CS8406 S/PDIF Audio Transmitter

The system generates standard S/PDIF data using a CS8406 192 kHz Digital Audio Transmitter. The CS8406 receives input data from the FPGA in PCM format and transmits S/PDIF data on both optical and coaxial output connectors. The optical output connector is limited to a maximum speed of 96 kHz. The coaxial connector supports Quad Speed 192 kHz clocking rates.

4.9 Serial Audio Interface

In addition to the standard S/PDIF outputs, the Customer Evaluation Board has been designed to allow Master and Slave operation using the Serial Audio Interface (SAI) via the 14-pin header, J4, which includes the signals MCLK, SCLK, LRCK, and the four serial data lines.

When the CS5364 is in Slave mode, SCLK and LRCK/FS must be supplied externally through the J4 header.

4.10 Analog Input Buffer

The CDB5364 includes an example of an active low-noise, single-ended-to-differential analog input buffer shown in the schematic drawings, Figures 10 and 11. Alternate active or passive, single-ended or differential topologies may be used as cost dictates. However, the high performance of the CS5364 may be compromised. Optimum device performance is met by buffering the CS5364 with a low noise structure that is stable with a 2700 pF output load.

5. SCHEMATICS

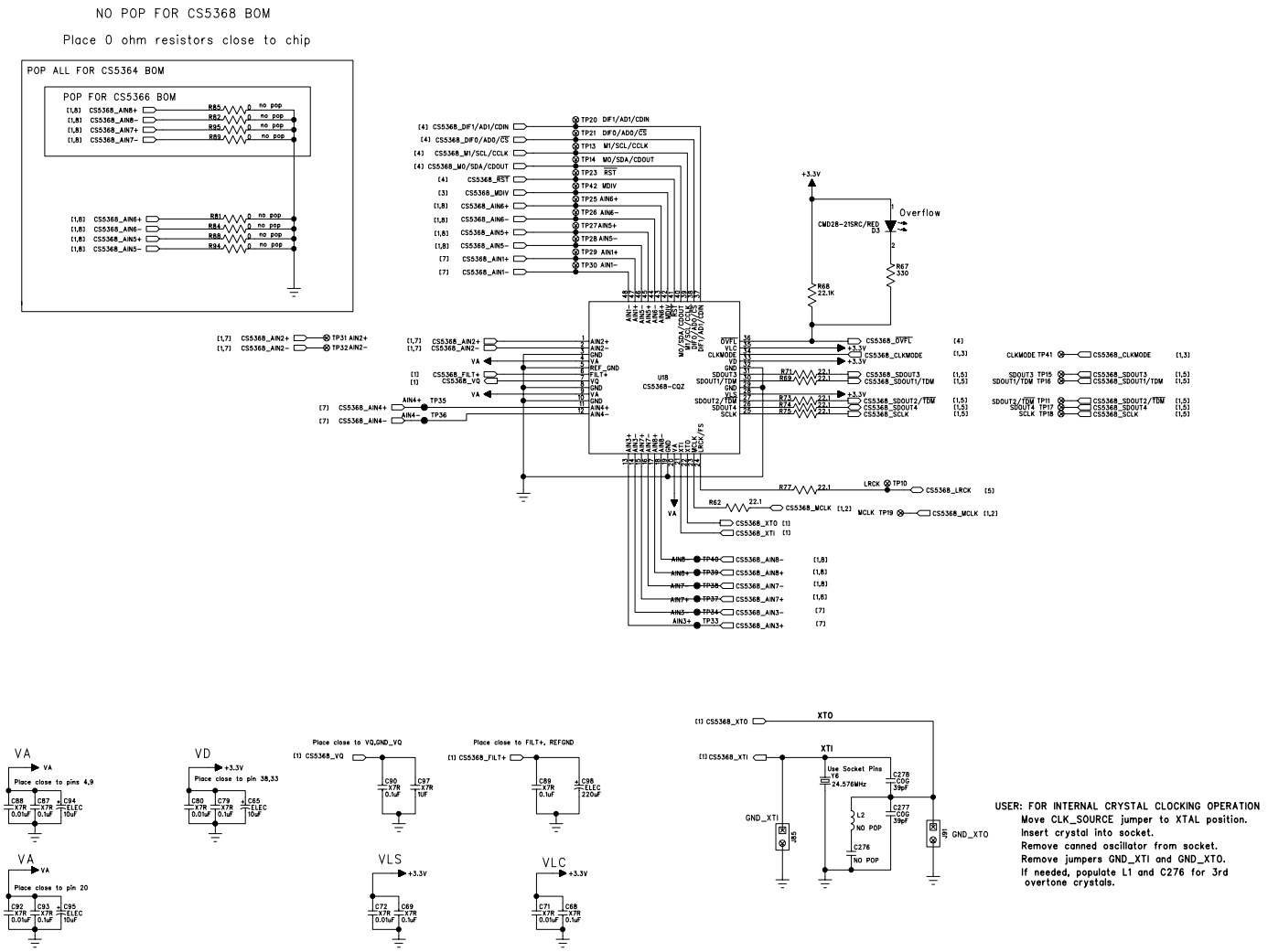

Figure 4. CS5364 (Schematic page 1)

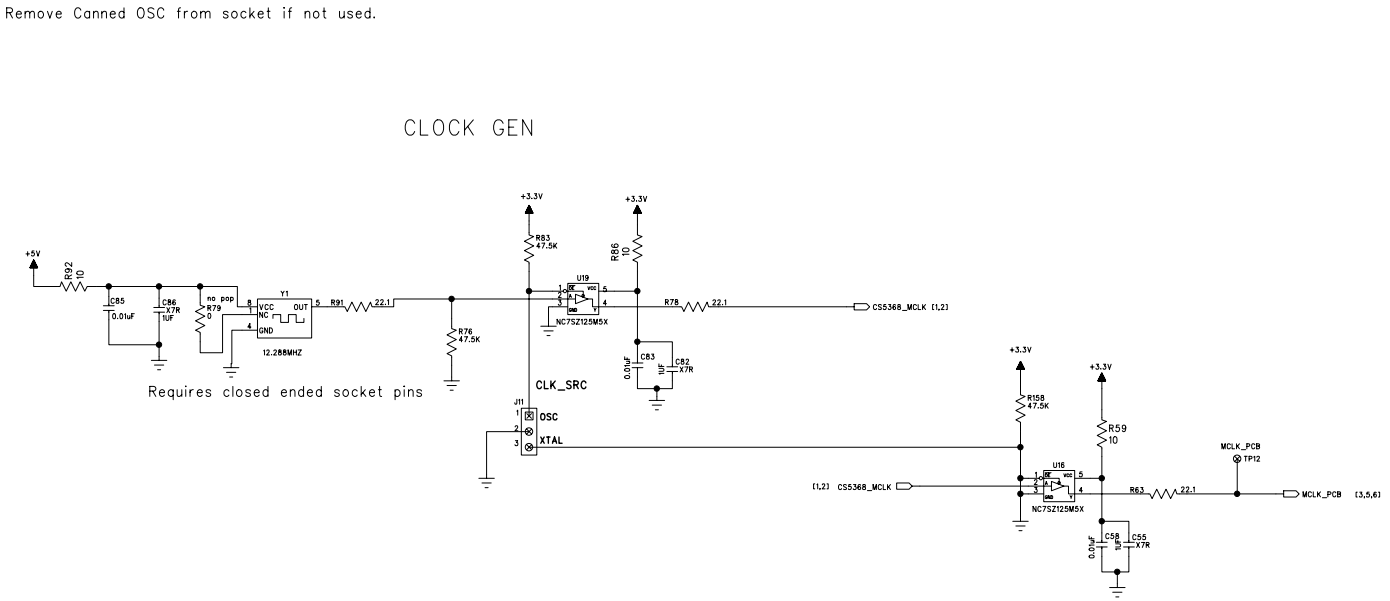

Figure 5. Clock Generation (Schematic page 2)

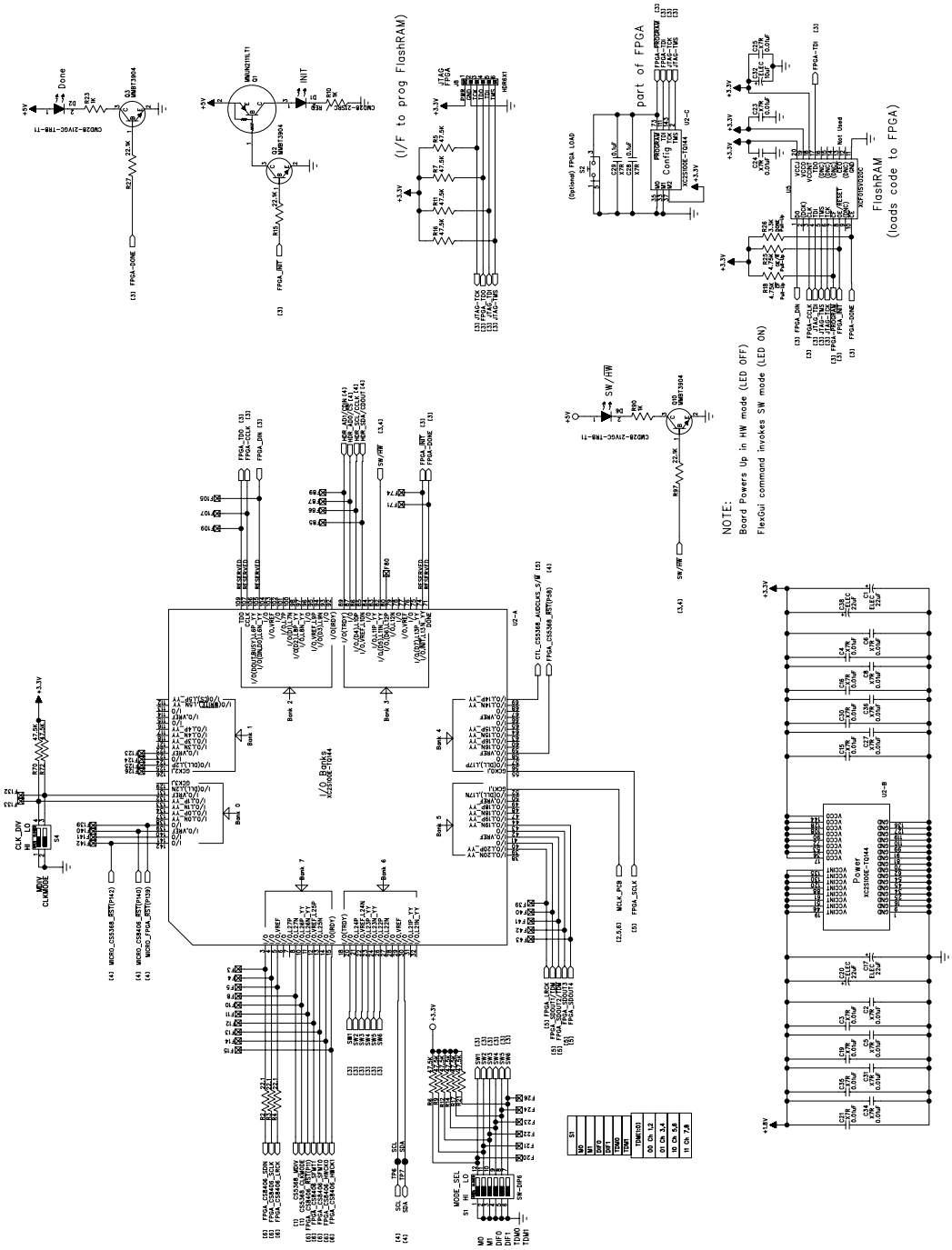

Figure 6. FPGA (Schematic page 3)

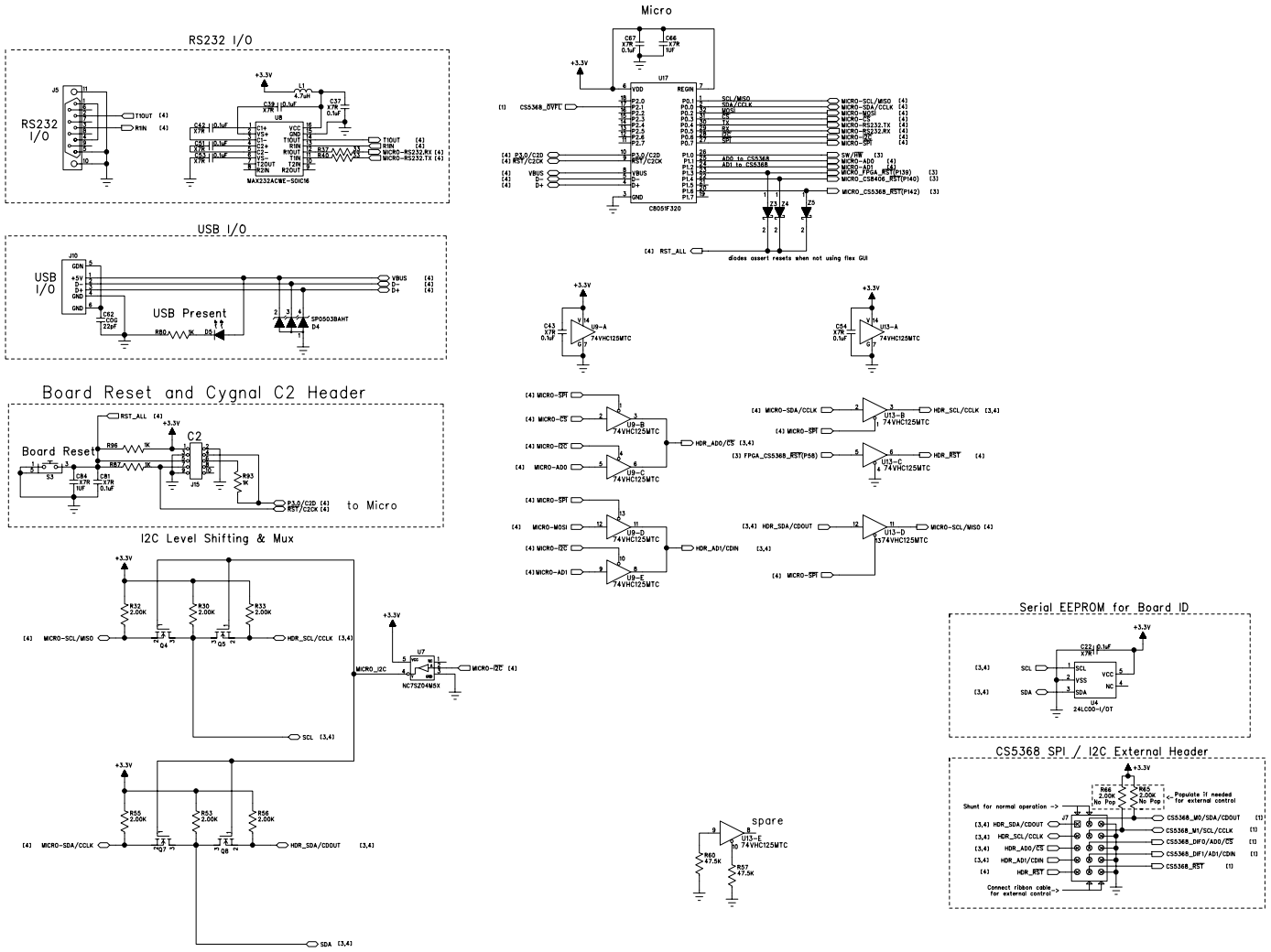

Figure 7. Control Port (Schematic page 4)

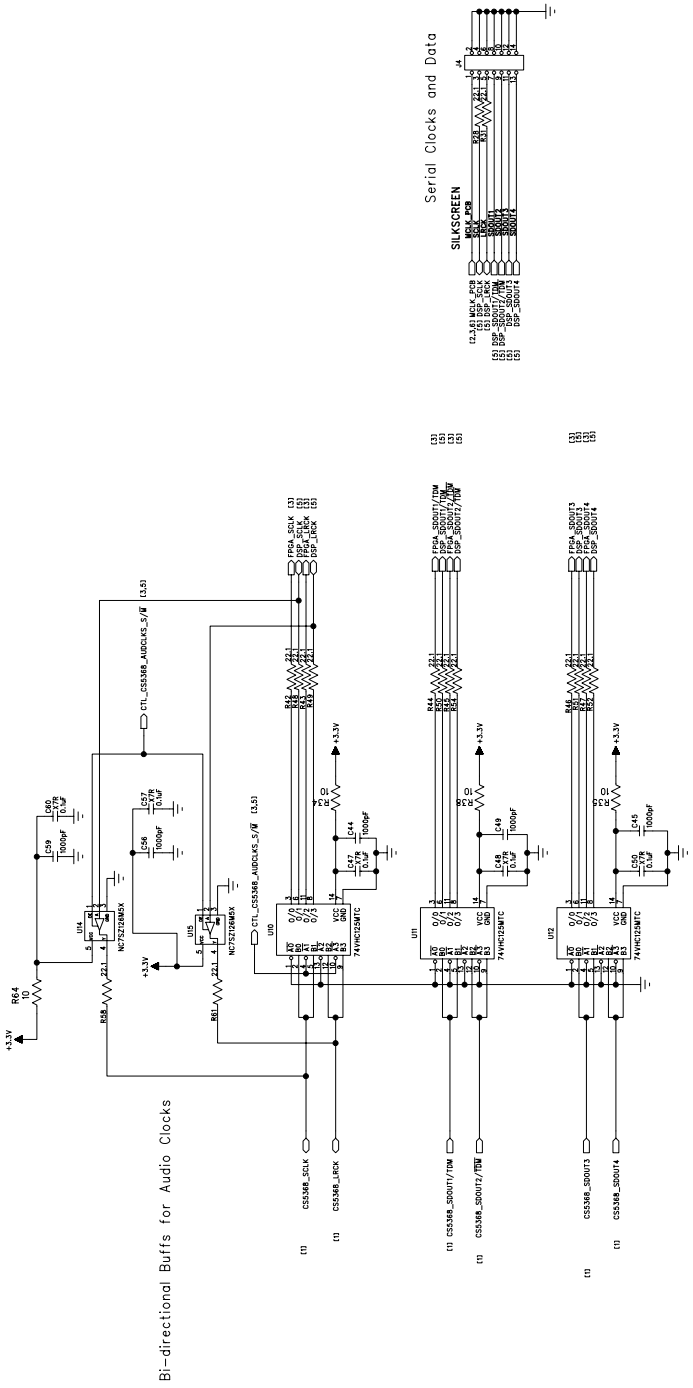

Figure 8. Clock and Data Buffers (Schematic page 5)

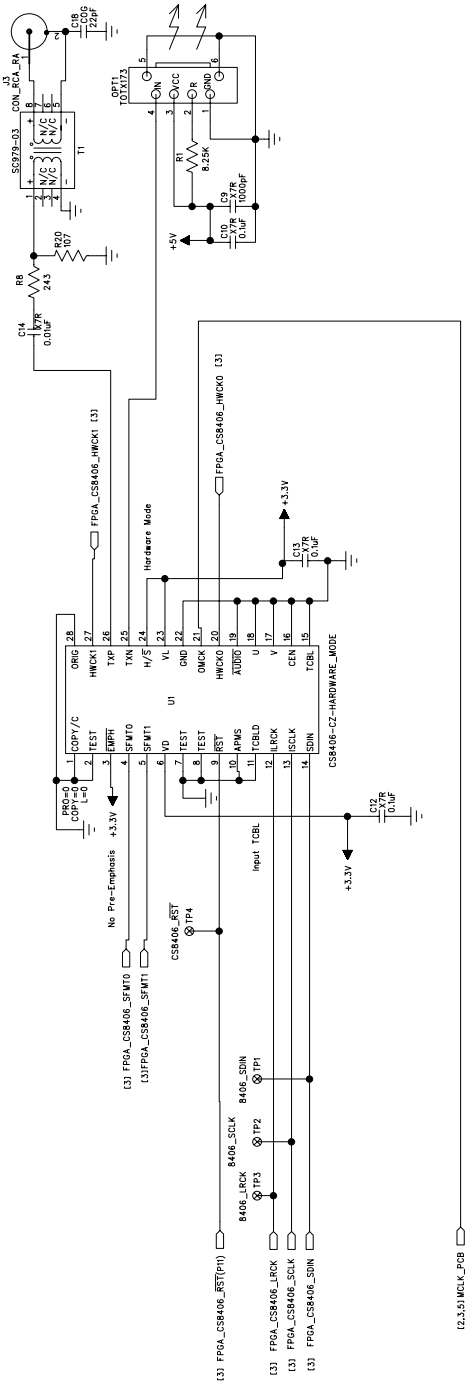

Figure 9. CD8406 S/PDIF Output (Schematic page 6)

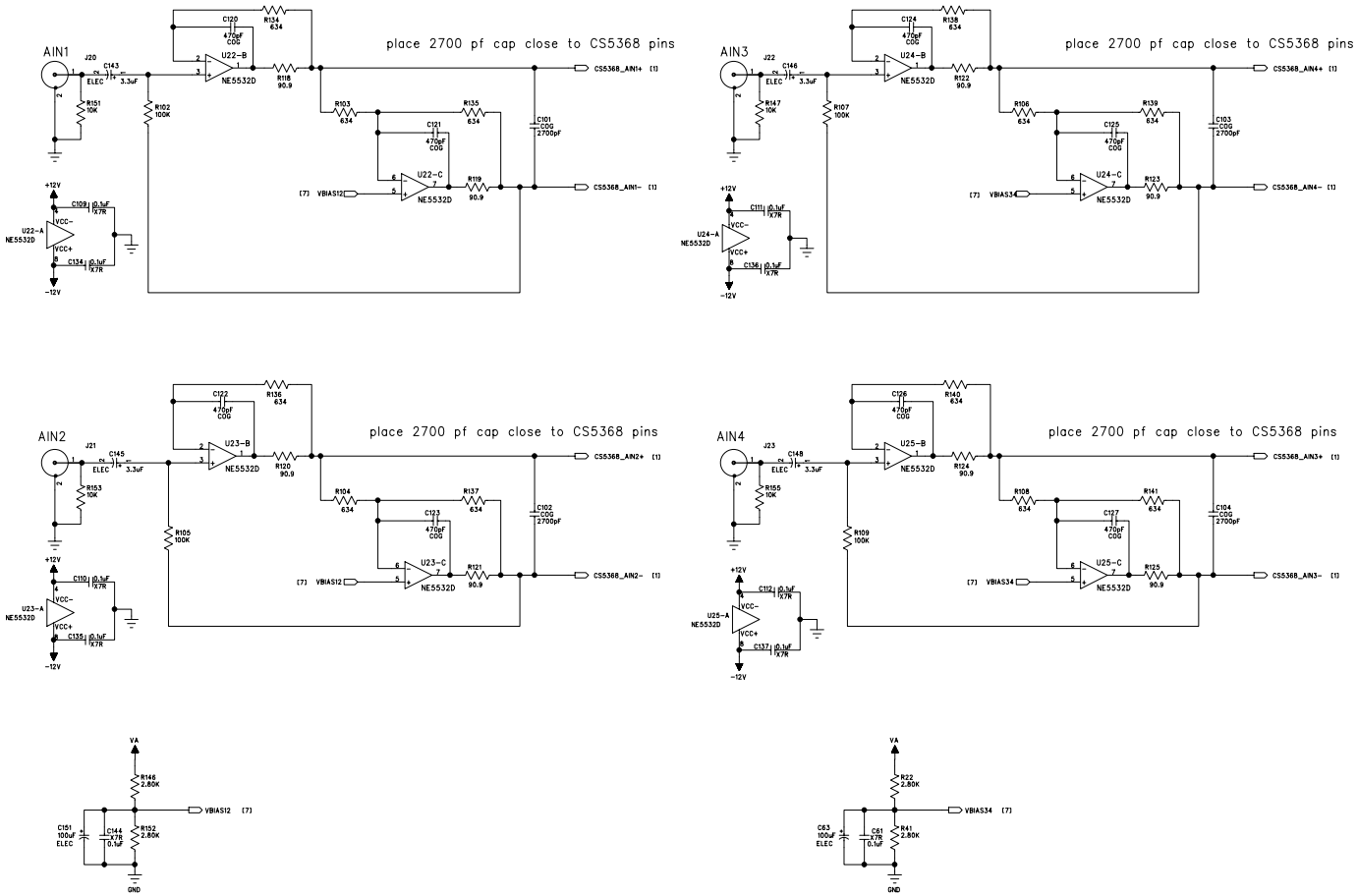

Figure 10. Analog Inputs 1 to 4 (Schematic page 7)

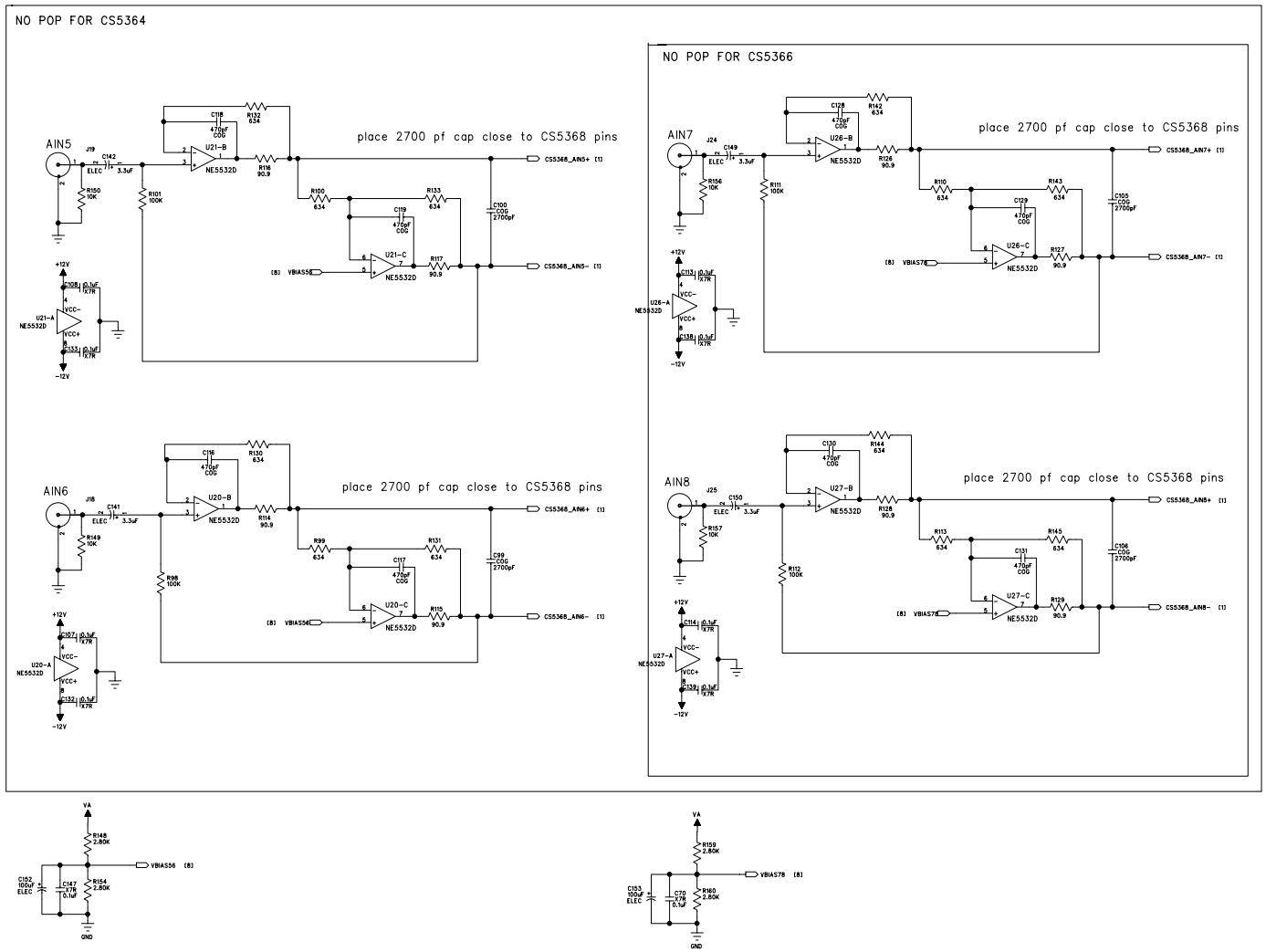

Figure 11. Analog Inputs 5 to 8 (Schematic page 8)

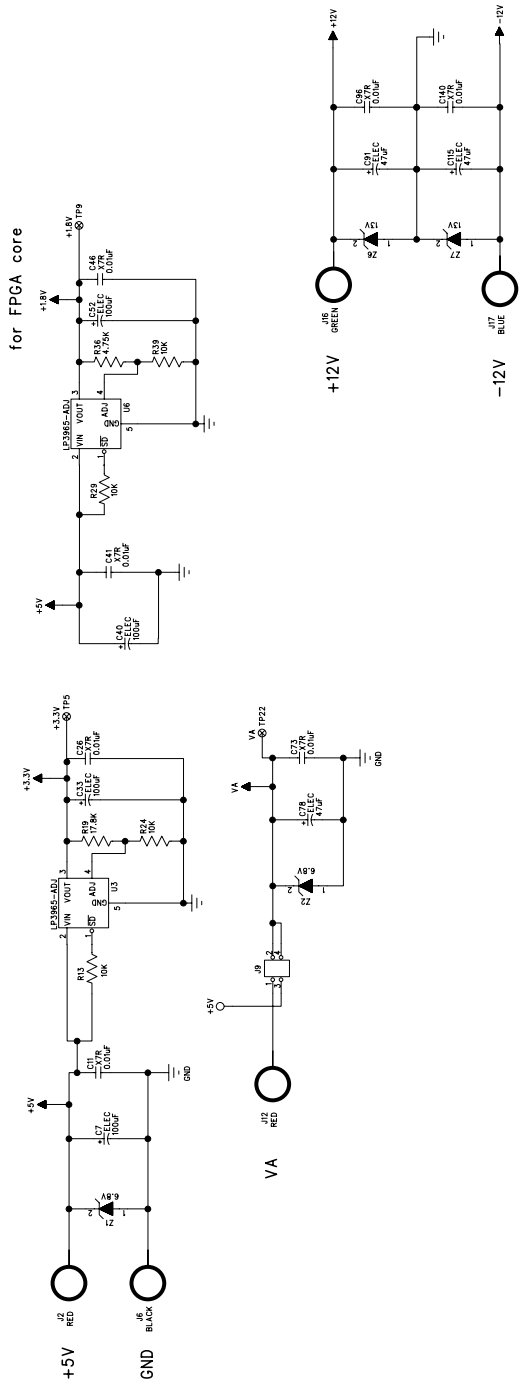

Figure 12. Power (Schematic page 9)

6. BOARD LAYOUT AND ROUTING PLOTS

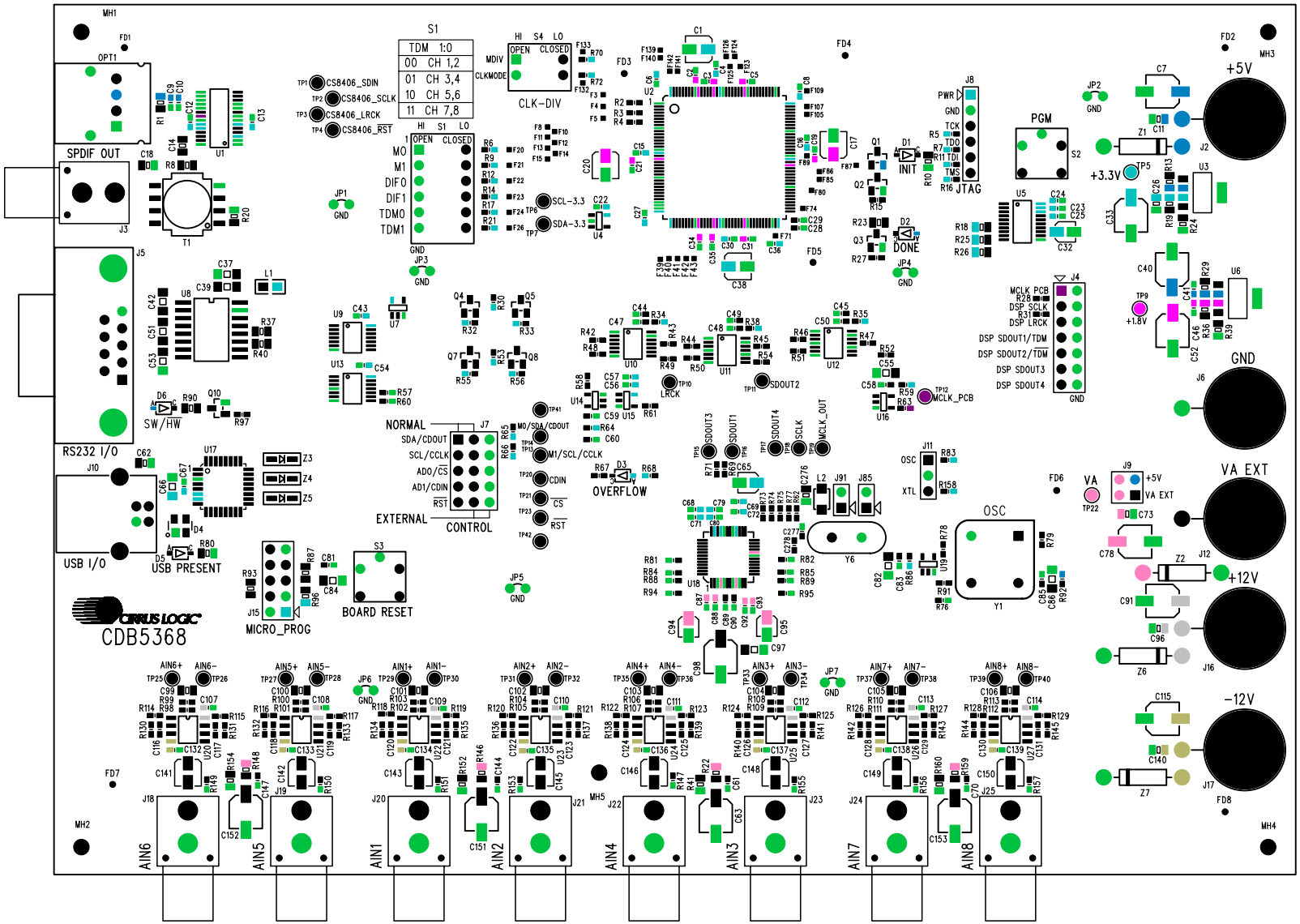

Figure 13. Top Silkscreen

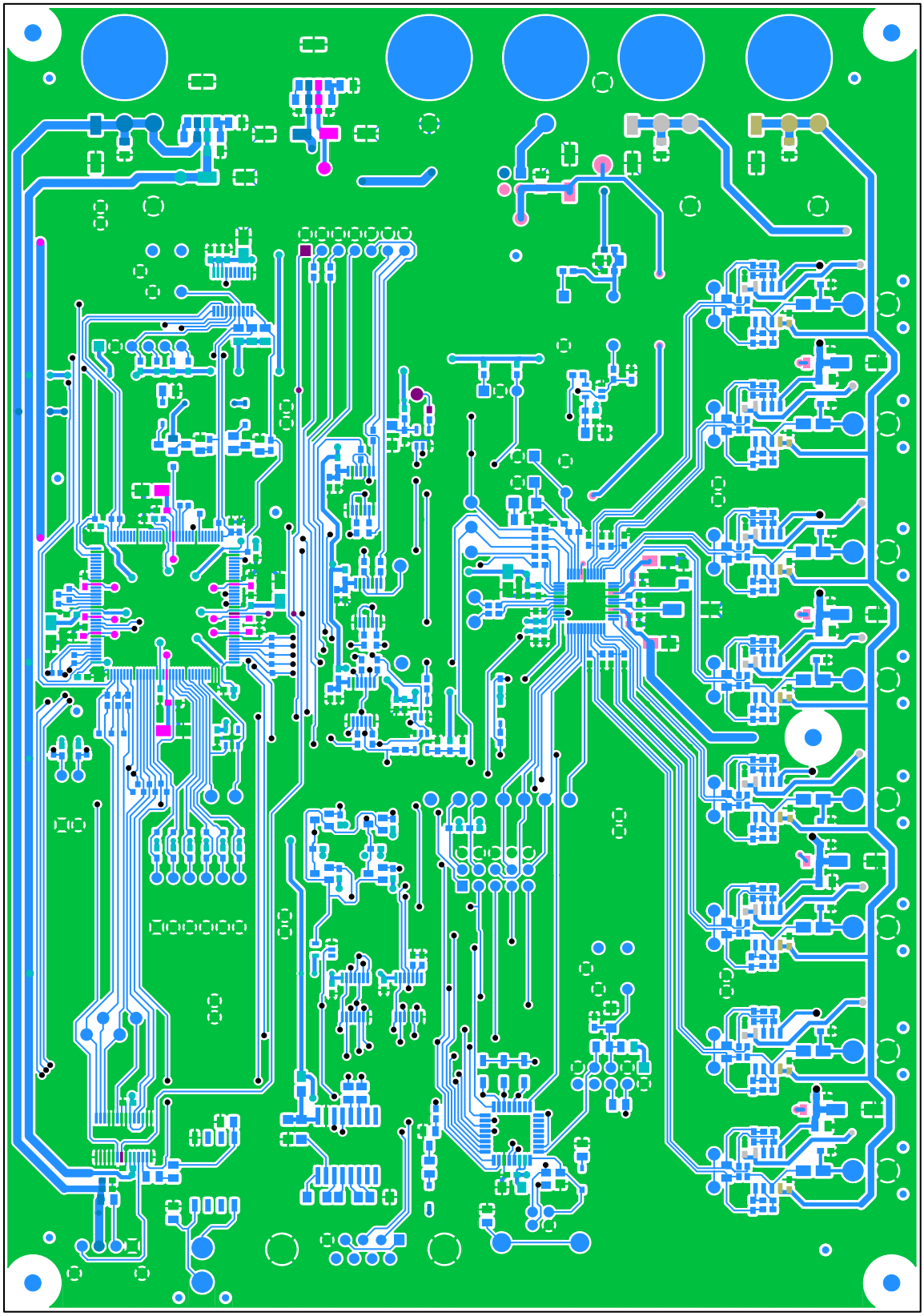

Figure 14. Top Layer

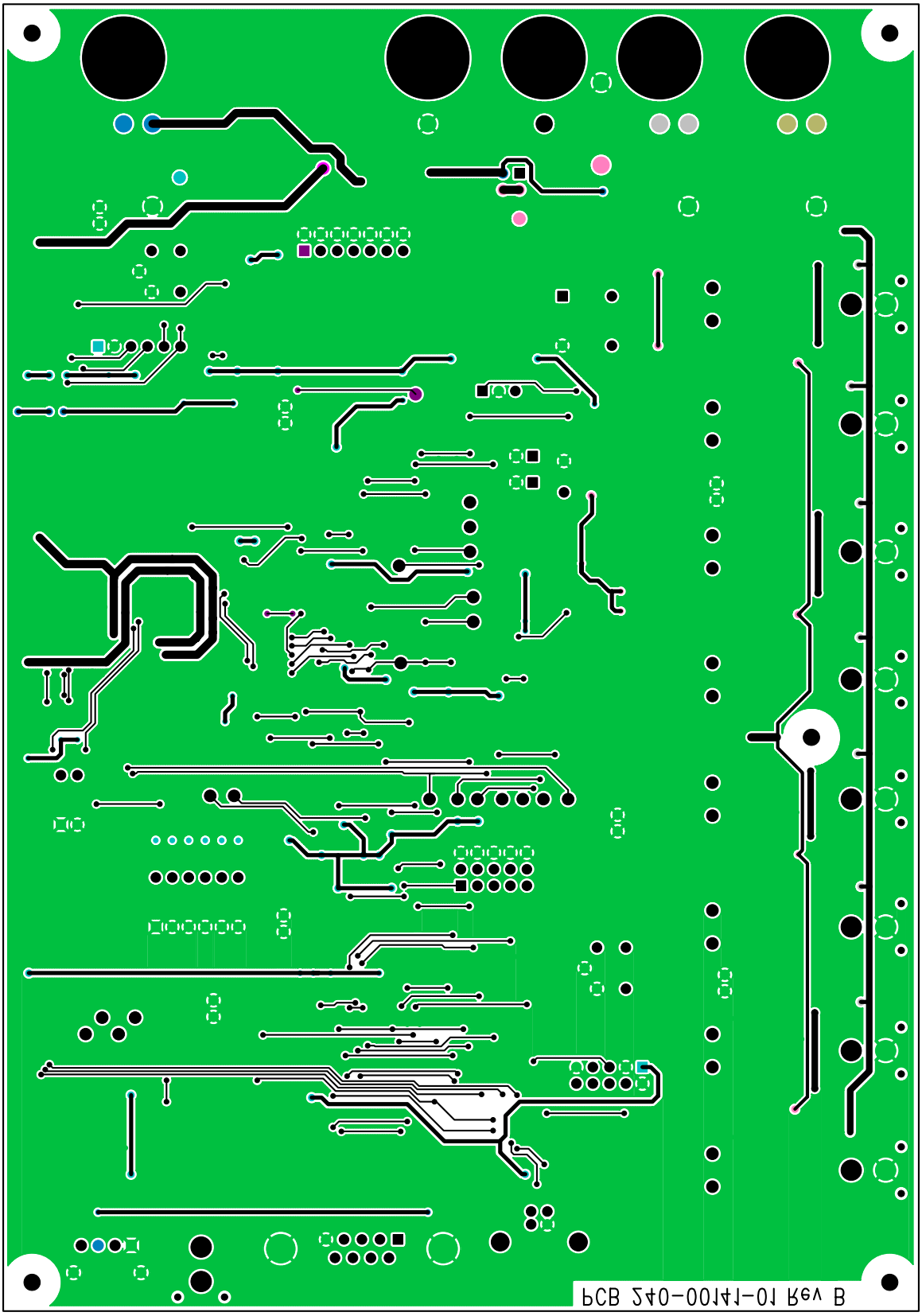

Figure 15. Bottom Layer

7. REVISION HISTORY

Release	Date	Changes
DB1	September 2005	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **<http://www.cirrus.com/corporate/contacts/sales.cfm>**